Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.117”**

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**.111”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .111” X .117” DATE: 11/16/21**

**MFG: MOTOROLA THICKNESS .015” P/N: MTC12N10E**

**DG 10.1.2**

#### Rev B, 7/1